MODEL RX-340 BLOCK DIAGRAM

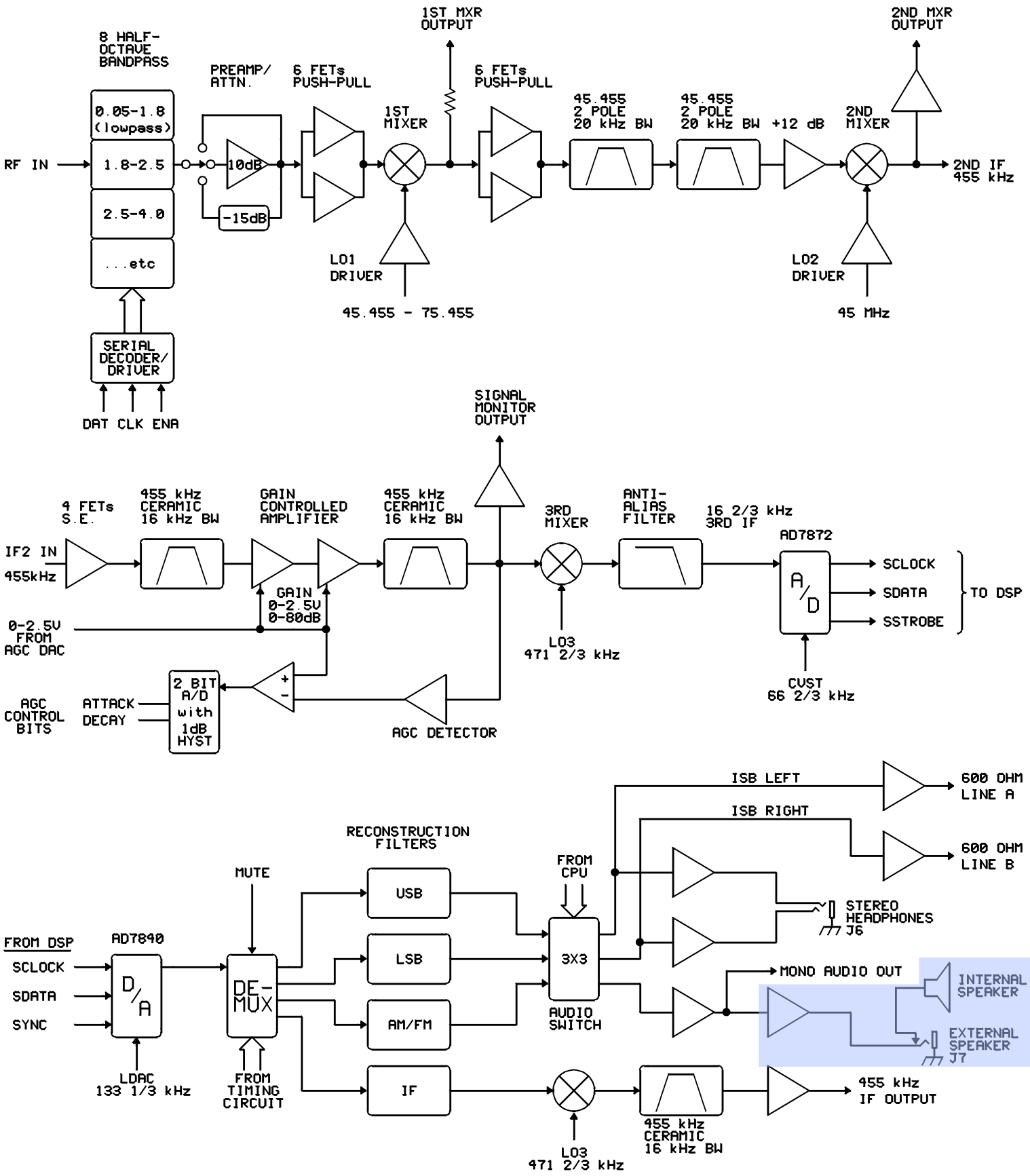


FIGURE 10-1

J5
ANTENNA
0.05 – 30 MHz

J9
1MX OUT
45.455 MHz

J10
2MX OUT
455 kHz

J3
SIG MON
455 kHz

J4
IF OUT
455 kHz

MONO AUDIO

STEREO PHONES

(PRESEL MUTE)

10 MHz

45.455 MHz

16 2/3 kHz

LO3
471 2/3 kHz

LO1 45.455 – 75.455 MHz

LO2 45 MHz

10 MHz

(LO2 SHUTDOWN)

PLL DATA

AGC A/D

AGC D/A

AGC CNTRL

A/D DATA

D/A DATA

AF SEL

AUDIO

J8
AUDIO
/ACCY

J8 PINOUT:
1 GND
2 MONO
3 LINE B–
4 B CT
5 LINE B+
6 LINE A–
7 A CT
8 LINE A+
9 GND
10 DC AUDIO
11 MUTE
12 USER 1
13 USER 2
14 USER 3
15 USER 4

81878
PRESELECTOR

81823.SMD
1ST MIXER

81817.SMD
2ND MIXER

81790.SMD
I/O

59 76 60 60 71 54 IF1 54 70 56 51 IF3 51 52 52 50 75 76 53 34 8 7 69 68 9 4 5 64 64 5 4 18 10 18 10 24 33 61 55 57 12 16 17 74 12 16 17 73

AC CPLD. AUDIO
DC CPLD. AUDIO
HARDWARE MUTE
600 OHM LINES

J2
EXT.REF.
1,2,5,10MHz

63

81772.TCXO
SYNTHESIZER

11,14 11,14 PLL DATA
25 25 SOL
15 15 REF SENSE,LOCK

81807
MAIN CPU / DSP

baud/bits B D P S
S1
iface I
addr A
S2
RS-232 CONFIG.SWITCHES

13 USER OUTPUTS

RS232

DATA OUT

PREAMP / ATTN. SEL. 33

FILTER SEL.

24

67 TX/SEL

81 72

J1 CONTROL/DATA
(PINOUT FIG. 5-4)

INTERNAL SPEAKER

EXTERNAL SPEAKER J7

93

SPEAKER VOLUME

I2C BUS

S-METER

STEREO HEADPHONES J6

PHONES VOLUME

96 94

+12
+5
-5
-12

TO ALL BOARDS

81824 FILTER
3

21200
POWER SUPPLY

2

POWER SWITCH

1

90-264 VAC

P1

POWER ENTRY MODULE

MAIN FREQUENCY DISPLAY

MAIN TUNING ENCODER

AUX.PARM. DISPLAY

82 84 88 81 72 95

AUX.EDIT ENCODER

89

MEM./SCAN DISPLAY

83

MEM.EDIT ENCODER

90

81819 FRONT PANEL CPU

8
34
97

SIGNAL STRENGTH METER

columns 85
rows 86
leds 87
gain 92

81820 KEYPAD BOARD

67

MANUAL GAIN CONTROL

LOGIC BOARD BLOCK DIAGRAM

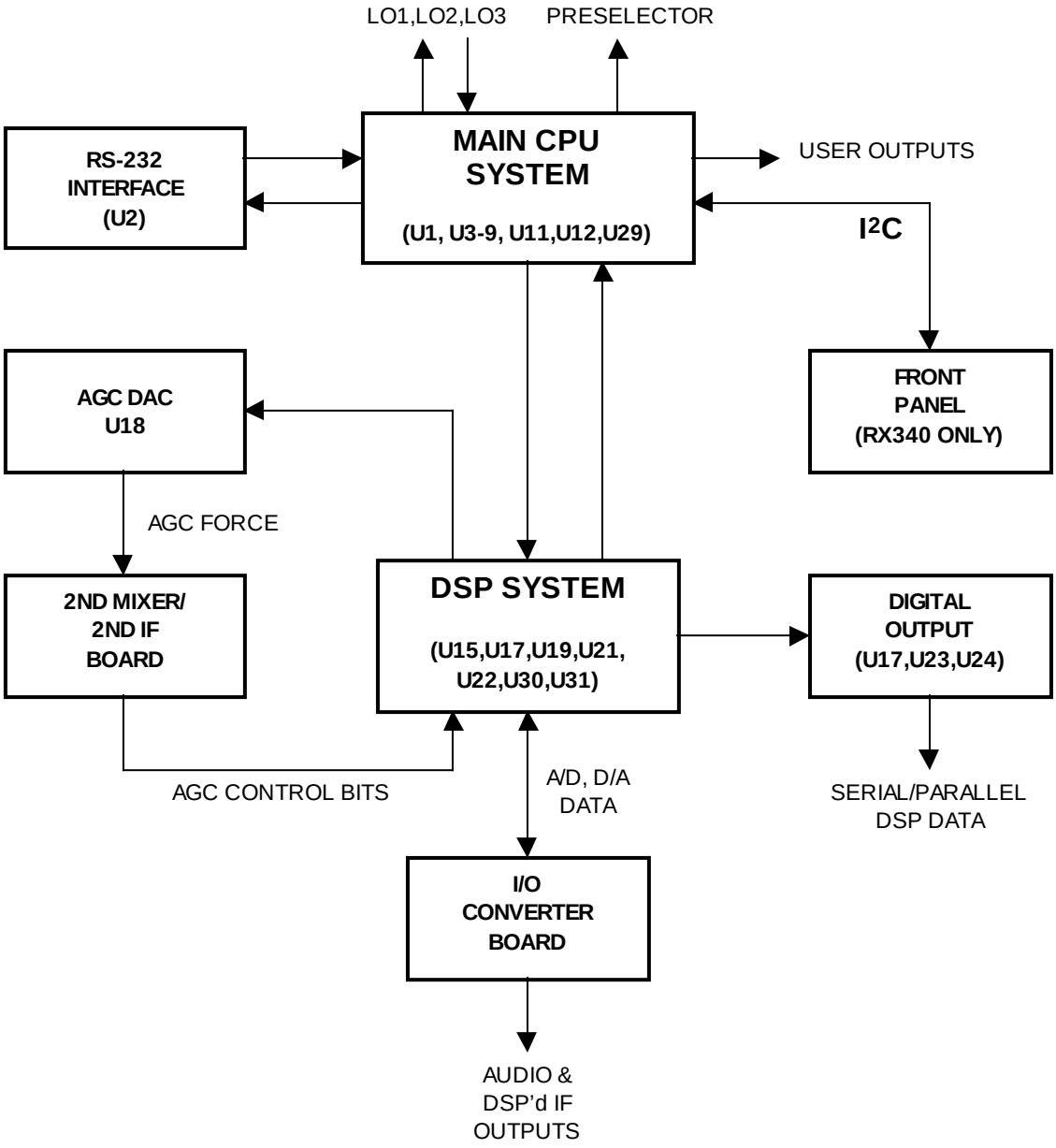


FIGURE 10-2

331/340 SYNTHESIZER BLOCK DIAGRAM

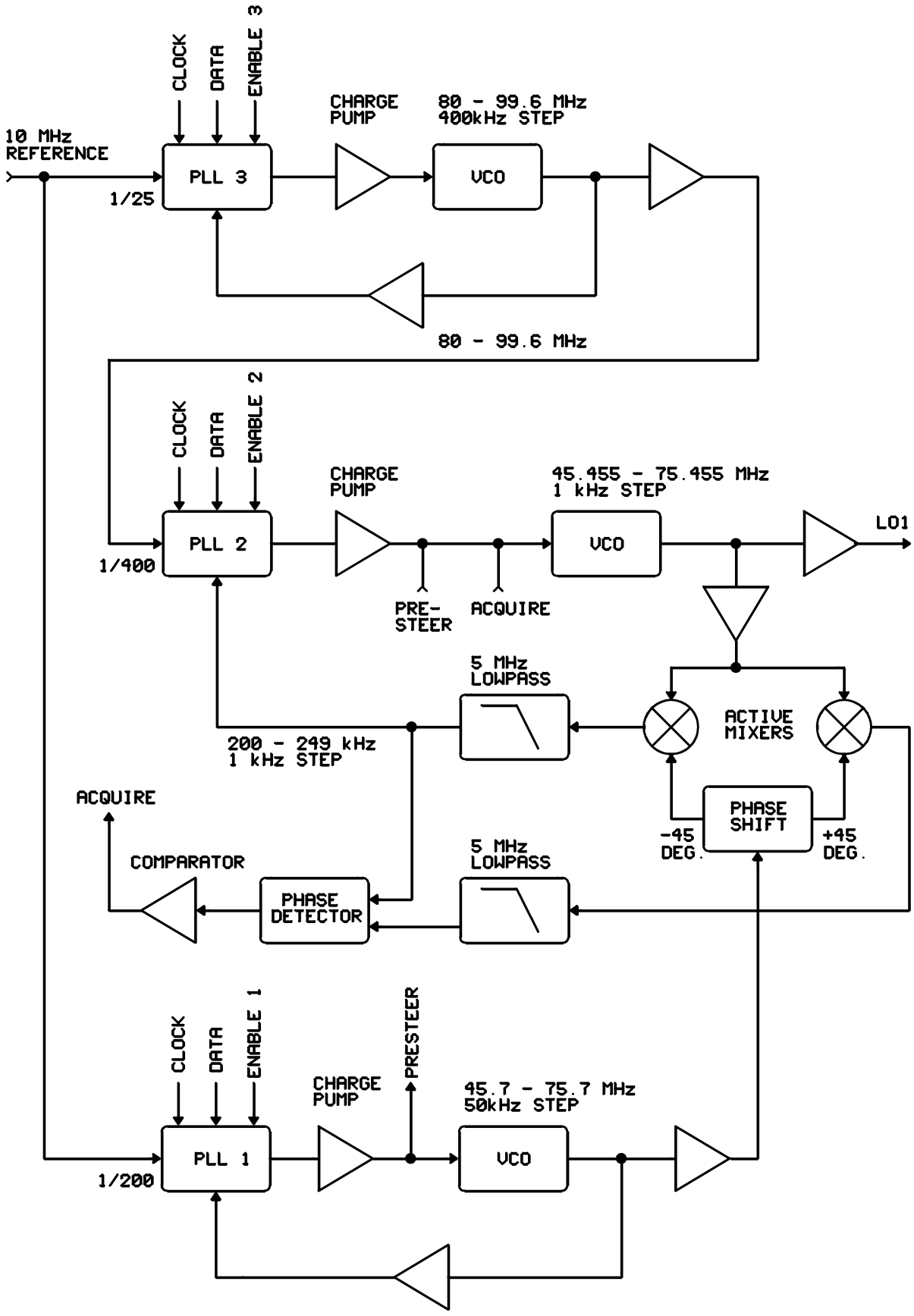


FIGURE 10-3

Technical Description of the RX331/340 analog AGC System

The 455 kHz analog IF amplifier provides most of the receiver's gain. The IF bandwidth is 20 kHz and an analog AGC loop with a fast natural time constant levels the IF amplifier's output to about 200 mV peak-to-peak over an 80 dB input range. The onset of this analog AGC is about 60 dB above the receiver's noise floor. The main purpose of this AGC loop is to protect the A/D converter from overload from strong signals. Weaker signal AGC is accomplished in the DSP (digital AGC) after the narrow bandwidth selectivity filtering.

The analog AGC needs to be overridden (set to lower gain) by the DSP in two cases, discussed below. The analog AGC also needs to be monitored by the DSP so it can make some fast gain corrections to the digital AGC. These digital gain corrections will be discussed after the two analog override cases.

First, when a medium or slow AGC decay rate is selected, the IF gain must return (after an analog AGC attack) at a controlled, slower than natural rate. This slower decay rate is necessary in cases such as SSB or low frequency AM modulation to prevent the fast analog AGC from "washing out" the modulation envelope. Also, this decay rate must be coordinated with the DSP's independent digital AGC to prevent a "double decay rate" phenomenon.

Second, for manual setting of less-than-maximum receiver gains, the analog AGC voltage must be overridden by a fixed voltage "ceiling" to place an upper bound on IF gain. For manual gain reduction, the digital gain is reduced first, and then the analog gain is reduced – preserving system noise figure at the lower gain settings.

This overriding control is accomplished with an op-amp circuit that "ORs" a D/A converter output with the naturally occurring analog AGC voltage. The op-amp circuit also develops two feedback bits that inform the DSP who is in control of the analog AGC at any instant – the analog AGC detector ("A" bit) or the D/A converter ("D" bit). These bits are used for two purposes: 1) coordination of analog and digital decay rates as mentioned in the first case above, and 2) correcting fast gain changes caused by large signals that are outside of the DSP selectivity filter passband. This second purpose is discussed below.

The operator expects AGC action only on signals that are inside the passband of the DSP selectivity filters – those signals he can "hear." These are called "in-band" signals. If a large signal exists outside the DSP passband, but inside the wider analog IF passband (the "out-of-band" signal), it will be unheard, but gain changes caused by the analog AGC action will cross-modulate the level of the in-band signal. Slow changes in gain due to this scenario will be followed (and corrected) by the DSP (digital) AGC. But a gain reduction that occurs at a rate faster than the selected AGC decay rate must be differentiated from a "real" drop in the level of the in-band signal. Left uncorrected, this artificial drop in receiver gain will punch an audible "hole" in the in-band signal until the digital AGC slowly decays to restore the signal level.

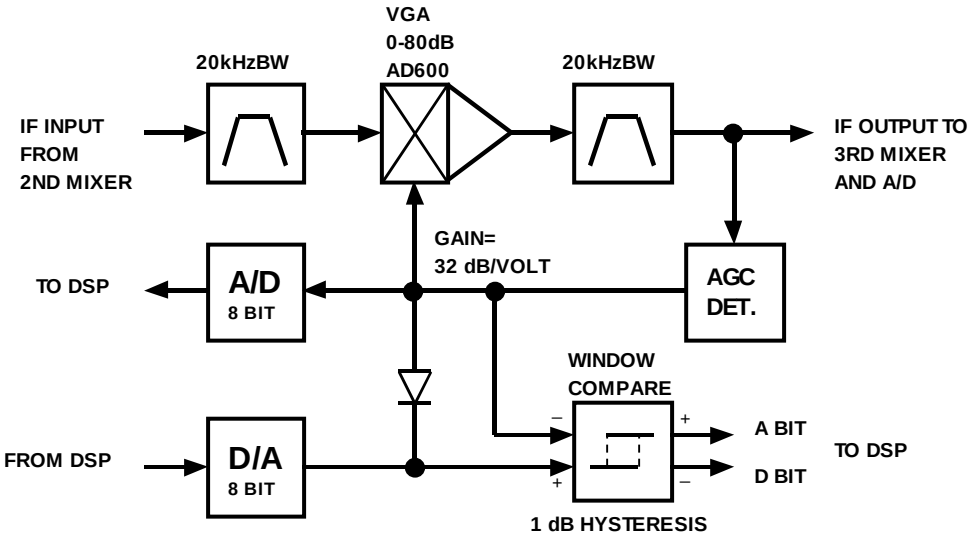
The logical differentiation between in-band and out-of-band caused gain reduction is accomplished by monitoring the “A” bit from the op-amp ORing circuit. Each time an “A” bit occurs, indicating analog AGC attack, an A/D converter on the analog AGC voltage is read and compared to the previous reading. The digital AGC is then allowed a fast decay only by the dB difference in the previous and present A/D values. This fast decay is only **allowed** and not forced, because it is only needed if the attack was caused by an out-of-band signal. If the attack was caused by the in-band signal, the “A” bit is the normal result of an increase in level of a strong desired signal, and no fast decay will be used because the in-band signal is already at (or very slightly above) the digital AGC attack threshold. As long as the “A” bit persists, the D/A is ramped down at the selected attack rate.

The “D” bit indicates that the D/A is controlling the analog AGC voltage instead of the AGC detector, and it is used to initiate a ramp-up of the D/A at the requested decay rate – simulating a decaying capacitor charge on the analog AGC line. As long as the “D” bit persists, the D/A continues ramping to its limit followed by increasing DSP gain (at the same rate) until full receiver gain is restored.

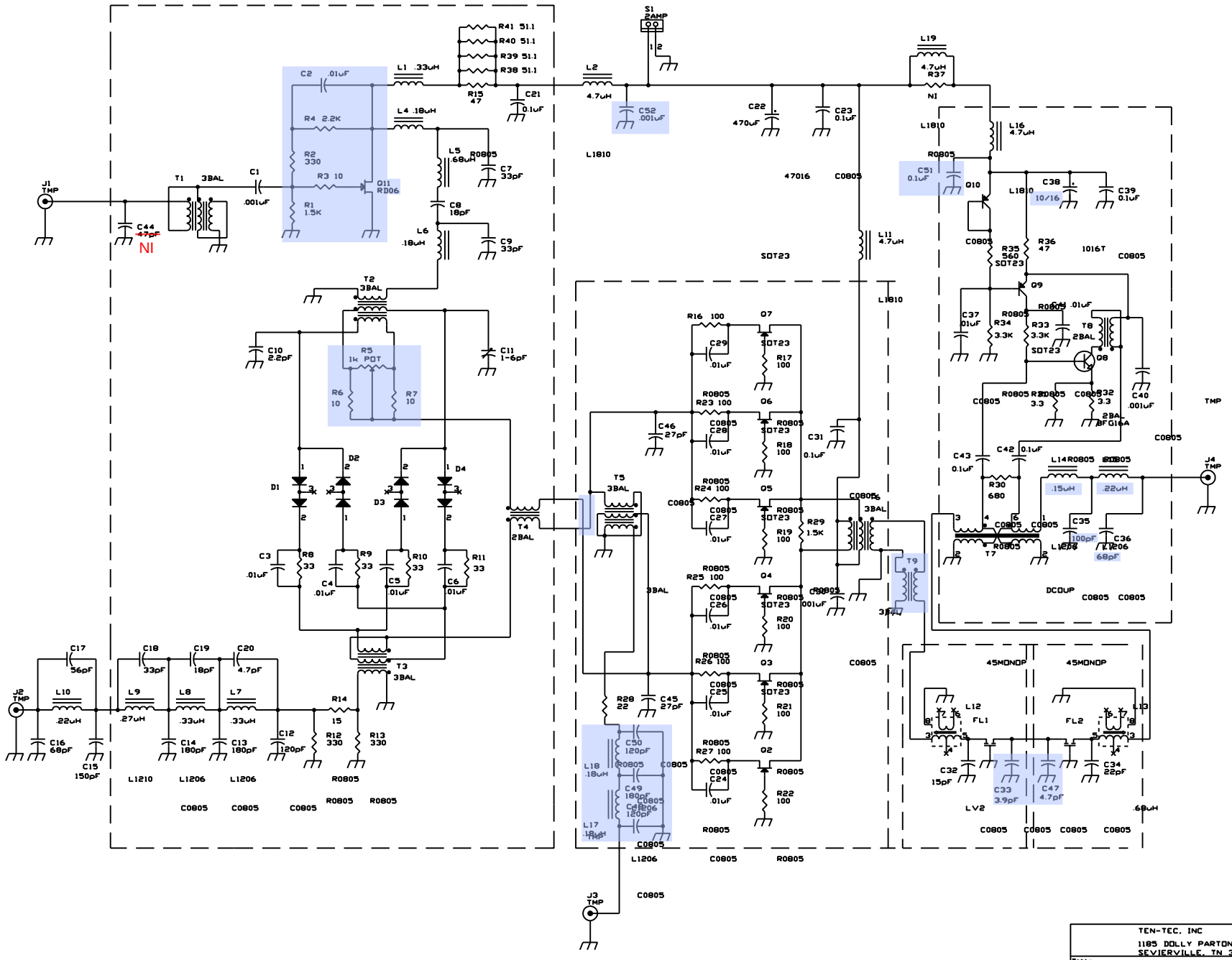
There is a 1 dB window where neither “A” nor “D” bit is expressed. This is considered the steady-state analog AGC voltage, and the D/A value is held constant. “A” and “D” bits never occur simultaneously.

Using a similar scheme in the RX400 will allow the feature of fully programmable AGC attack, hang, and decay rates in addition to improved cross-modulation performance due to the out-of-band AGC correction.

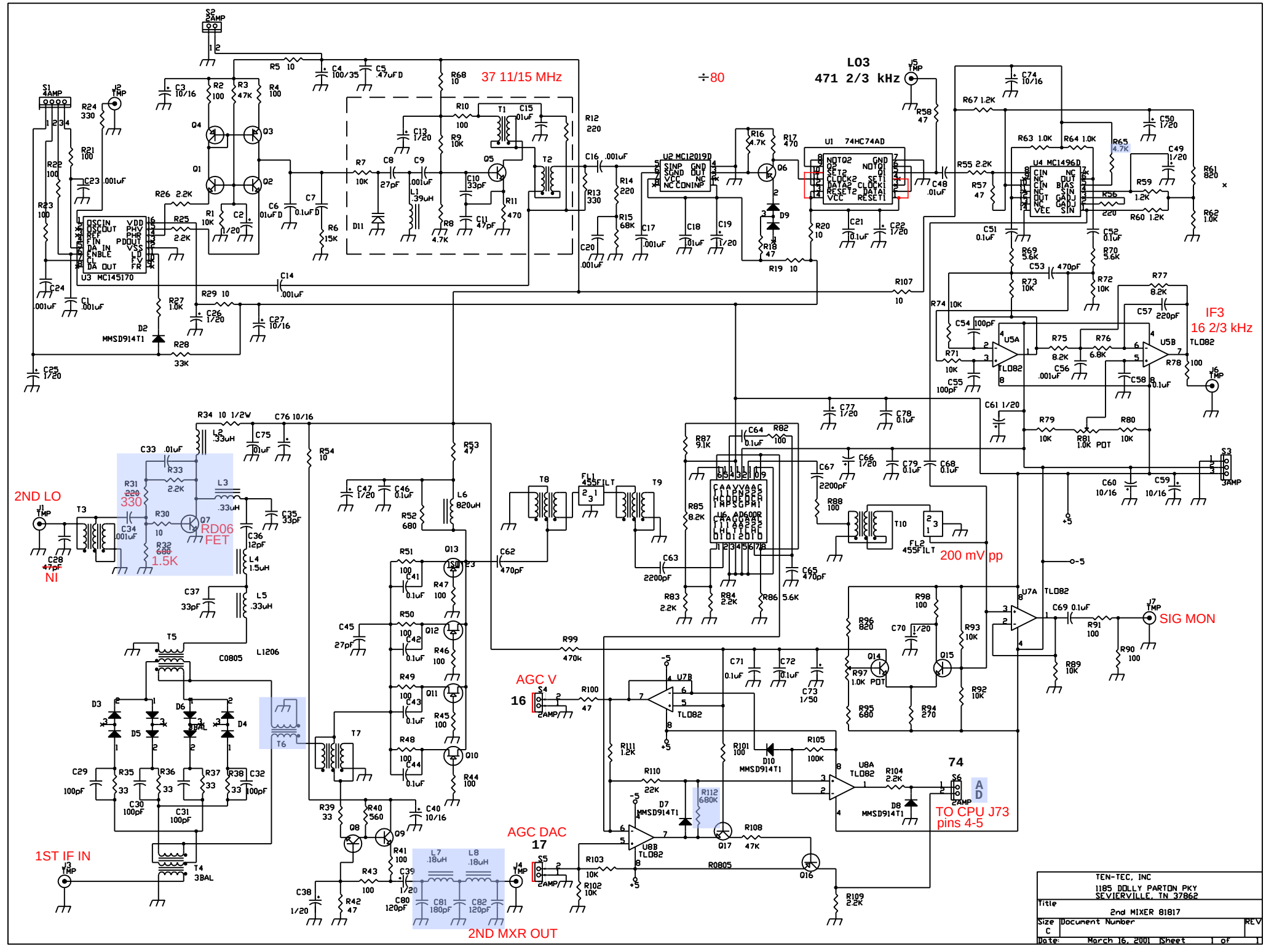
Note: The AD8367 is an improved version of the AD600 VGA, useable to 500 MHz. I would recommend placing most of the receiver gain at 21.4 MHz though, where the 300-500 kHz bandwidth would reduce the number of “out-of-band” signals.

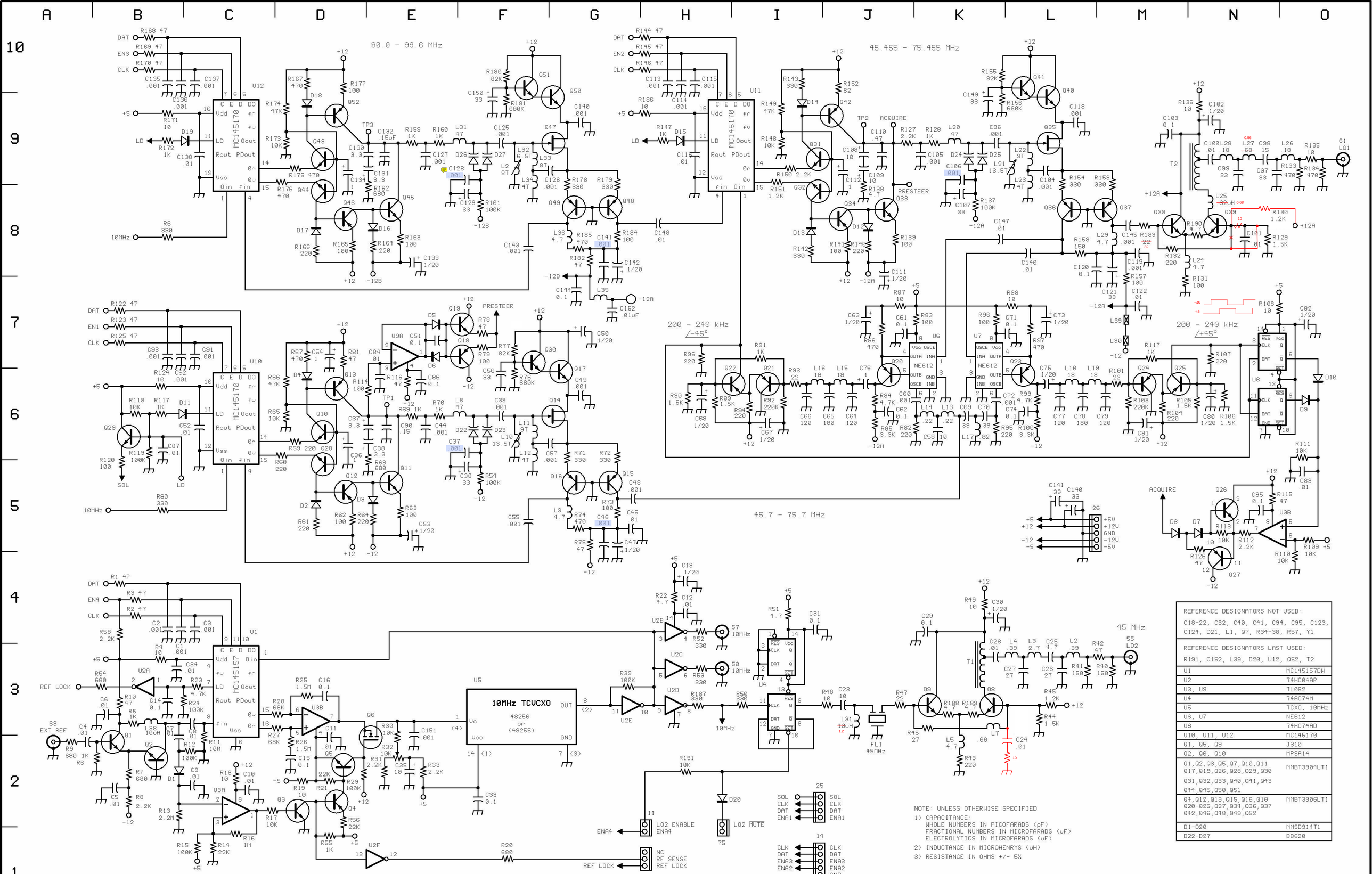


RX331/340 ANALOG AGC CONTROL SYSTEM



TEN-TEC, INC 1185 DOLLY PARTON PKY SEVIERVILLE, TN 37862		
Title: 1st Mixer Board 81823S		
Size: C	Document Number	REV
Date: August 20, 2005	Sheet 1 of 1	


37 11/15 MHz
÷80
L03
471 2/3 kHz
IF3
16 2/3 kHz
2ND LO
330
RD06
FET
1.5K
NI
200 mV pp
SIG MON
AGC V
16
AGC DAC
17
74
TO CPU J73
pins 4-5
1ST IF IN
2ND MXR OUT
U3 MC145170
U1 74HC74AD
U2 MC12019D
U4 MC1496D
TL082
MMSD914T1
TEN-TEC, INC
1185 DOLLY PARTON PKY
SEVIERVILLE, TN 37862
2nd MIXER 81817
March 16, 2001


80.0 - 99.6 MHz
45.455 - 75.455 MHz
45.7 - 75.7 MHz
200 - 249 kHz
/-45°
200 - 249 kHz
/+45°
45 MHz
10MHz TCVCXO
48256
or
(48255)
PRESTEER
ACQUIRE
REFERENCE DESIGNATORS NOT USED:
C18-22, C32, C40, C41, C94, C95, C123, C124, D21, L1, Q7, R34-38, R57, Y1
REFERENCE DESIGNATORS LAST USED:
R191, C152, L39, D20, U12, Q52, T2
U1 MC145157DW
U2 74HC04AP
U3, U9 TL082
U4 74AC74M
U5 TCXO, 10MHz
U6, U7 NE612
U8 74HC74AD
U10, U11, U12 MC145170
Q1, Q5, Q9 J310
Q2, Q6, Q10 MPSA14
Q1,Q2,Q3,Q5,Q7,Q10,Q11 Q17,Q19,Q26,Q28,Q29,Q30 Q31,Q32,Q33,Q40,Q41,Q43 Q44,Q45,Q50,Q51 MMBT3904LT1
Q4,Q12,Q13,Q15,Q16,Q18 Q20-Q25,Q27,Q34,Q36,Q37 Q42,Q46,Q48,Q49,Q52 MMBT3906LT1
D1-D20 MMSD914T1
D22-D27 BB620
NOTE: UNLESS OTHERWISE SPECIFIED
1) CAPACITANCE:
WHOLE NUMBERS IN PICOFARADS (pF)
FRACTIONAL NUMBERS IN MICROFARADS (uF)
ELECTROLYTICS IN MICROFARADS (uF)
2) INDUCTANCE IN MICROHENRYS (uH)
3) RESISTANCE IN OHMS +/- 5%
12/19/00
SYNTHESIZER
81772.TCXO